Grain Boundary Effects on the Mobility of Chemical Vapor Deposition Synthesized Monolayer MoS_2-FETs①

JU Qian-Kun[a, b] HONG Wen-Ting[a, b] LIU Wei[a, b, c]②

[a] (*CAS Key Laboratory of Design and Assembly of Functional Nanostructures, and Fujian Provincial Key Laboratory of Nanomaterials, Fujian Institute of Research on the Structure of Matter, Chinese Academy of Sciences, Fuzhou* 350002, *China*)

[b] (*University of Chinese Academy of Sciences, Beijing* 100049, *China*)

[c] (*Fujian Science & Technology Innovation Laboratory for Optoelectronic Information of China, Fuzhou* 350108, *China*)

ABSTRACT Molybdenum disulphide (MoS_2) has emerged as a promising candidate for low-power digital applications. However, grain boundaries play a decisive role in determining the carrier mobility and performance of MoS_2-FETs. In this work, we report a systematic study on the grain boundary of chemical vapor deposition (CVD) MoS_2. We found that in the ON-state, if current flows across a grain boundary that is aligned perpendicular to the channel length, the current of CVD MoS_2-FETs can be significantly reduced, while in the OFF-state, the effect is negligible. Metal-insulator-transition is clearly observed, indicating the high quality of our CVD samples, and it is also shown that grain boundaries increase the metal-insulator-transition crossover-voltage in MoS_2-FETs. Thereby, this work provides useful information and guidance in understanding the nature of carrier transport in synthesized MoS_2 devices, and the developed framework can be applied to other 2*D* semiconductors in general, as well as in optimizing the CVD process and device design with 2*D* materials.

Keywords: grain boundary, golybdenum disulfide, ghemical vapor deposition, field-effect transistor;

DOI: 10.14102/j.cnki.0254–5861.2011–2934

1 INTRODUCTION

Atomically-thin molybdenum disulphide (MoS_2) has emerged as a promising candidate for low-power digital applications[1-7]. The development of chemical vapor deposition (CVD) technology in the synthesis of large-area monolayer MoS_2 enables the possibility of fabricating entire digital circuits and systems on MoS_2[8-15]. However, the current synthesis techniques can only grow individual MoS_2 domains or polycrystalline MoS_2 films on dielectric substrates[8-15]. If grain boundaries exist in the channel of a field-effect transistor (FET), the imperfection sites will induce extra scattering, thereby causing variations in the device performance. Hence, grain boundary effects on the electrical properties of MoS_2 film can not be ignored. Although the effects of grain boundaries on the performance of CVD MoS_2-FETs have been noticed in few works[14-16], there is a lack of comprehensive study of grain boundary effects on the performance of CVD monolayer MoS_2-FETs. Recently, Ly et al. observed misorientation-angle-dependent electrical property of CVD MoS_2 film[17]. However, since a grain boundary may consist of many types of orientations (or angles), it is desirable to study the mechanism of grain boundary effects on the carrier transport in high-quality MoS_2 samples. This study will be helpful in optimizing the design and performance of MoS_2 for nanoscale electronic and optoelectronic devices. Such study is also critical for optimizing the CVD process for emerging 2*D* materials including MoS_2. In this paper, combining abinitio theoretical calculations with carefully designed experiments, we report a systematic approach to understand grain boundary effects on the performance of monolayer MoS_2-FETs on CVD synthesized high-quality samples.

Received 3 July 2020; accepted 1 September 2020

① This work was supported by the National Natural Science Foundation of China (No. 61674152)

② Corresponding author. E-mail: liuw@fjirsm.ac.cn

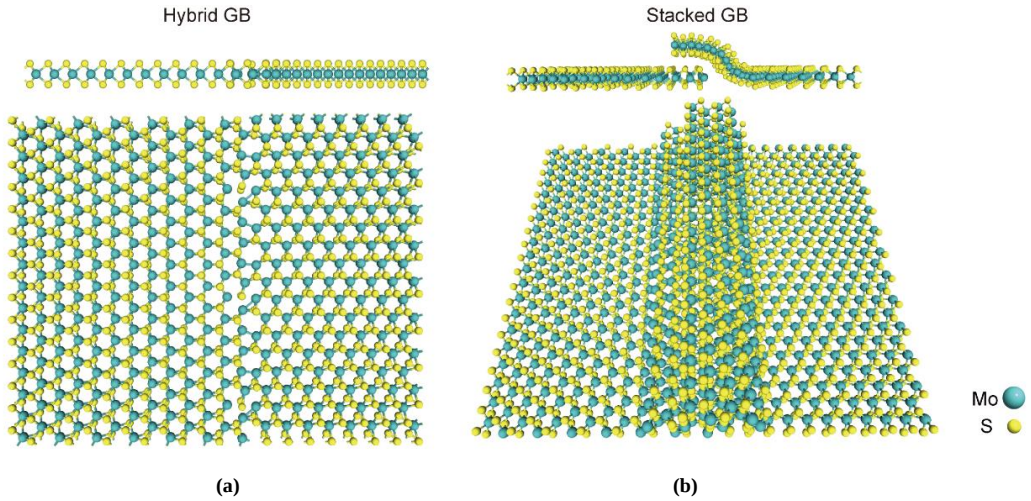


Fig. 1. (a) Side and top views of the schematic of a prototype hybrid grain boundary between two monolayer MoS_2 films. In this example, the GB consists of zigzag and armchair geometries. (b) Side and top views of the schematic of a stacked GB formed between two monolayer MoS_2 films. The two pieces of MoS_2 climb over each other during the growth

In general, there are two types of grain boundaries found in the CVD synthesized MoS_2 films, as shown in Fig. 1. In large MoS_2 films, stacked grain boundaries are more common than hybrid grain boundaries (indicated by the red arrows in Fig. 2a). However, in CVD individual domains, the hybrid grain boundary can be distinguished by the shape and orientation of the edge of MoS_2 domains. Once the individual domains merged into an entire MoS_2 film, hybrid grain boundaries can not be easily distinguished, while stacked grain boundaries can be easily avoided for device fabrication due to the distinct optical contrast. Then, hybrid grain boundaries may influence the performance of MoS_2 devices. Hence, in this work, device fabrication and theoretical calculations are performed based on the hybrid grain boundary to accurately collect the information of grain boundary effect on the carrier transport.

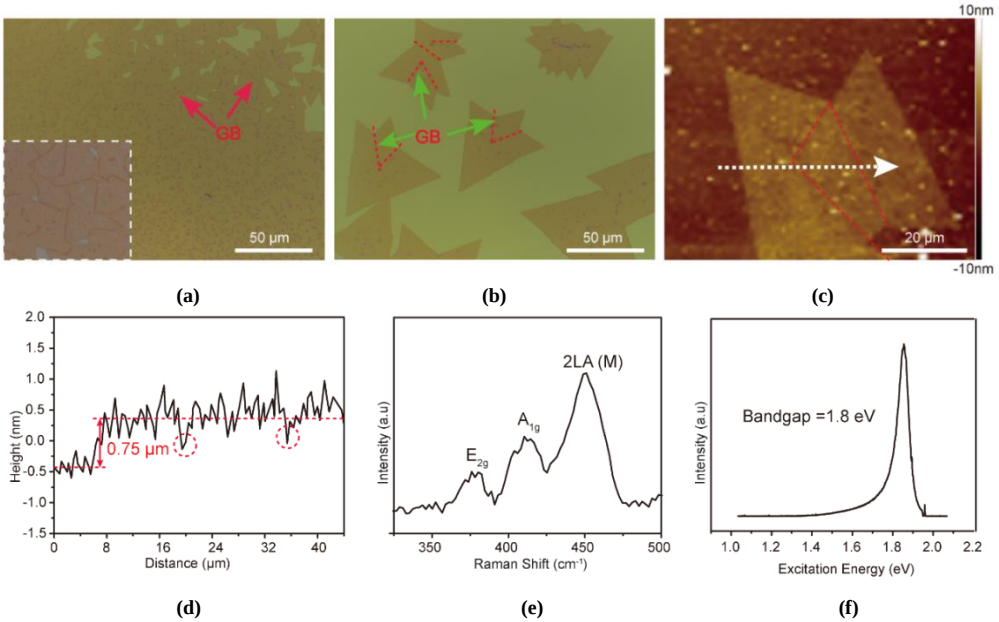


Fig. 2. (a) Low magnification optical microscope image of the monolayer MoS_2 film synthesized by CVD. Dark dots and lines indicate the grain boundaries, which are indicated by the red arrows. Inset shows a large magnification optical microscope image. Dark lines are stacked grain boundaries. (b) High magnification optical microscope image of the individual domains. The grain boundaries are illustrated by the red dash lines. (c) AFM image near the grain boundary. The red dotted line identifies the grain boundary. (d) The AFM line height profile along the direction of the white arrow in Fig. 2(c), indicating that the sample thickness is 0.75 nm. At the same time, a significant decrease in the thickness at the grain boundaries was observed. (e) Raman spectra of our synthesized monolayer MoS_2. Raman laser wavelength: 633 nm. 2LA(M) is a second-order Raman mode due to LA phonons at the M point in the Brillouin zone. (f) Photoluminescence spectra of monolayer CVD MoS_2

2 EXPERIMENTAL

2. 1 CVD synthesis of MoS_2 monolayer

In this work, monolayer (1L) MoS_2 is grown by vapor transport synthesis from solid powder precursors. High purity MoO_3 (99.5%, 5 mg) powder and SiO_2 (280 nm)/Si wafer as the growth substrate were placed in separate alumina boats and were loaded in the center of a 2 in diameter quartz-tube furnace. The boat with sulfur (≥ 99.5%, 200 mg) powder was placed 20 cm away from the center of the tube furnace. For the MoS_2 monolayer growth, the center of the furnace was heated to 750 ℃ for 10 min with the flow of 200 sccm Ar. After growth, the system was cooled down to room temperature while flowing with 500 sccm Ar. Fig. 2a is the low magnification optical microscope image of monolayer MoS_2 film synthesized by CVD. Dark dots and lines indicate the grain boundaries, which are indicated by the red arrows. Inset shows a large magnification optical microscope image. The grain boundaries are also marked by the red dashed lines on the individual monolayer MoS_2 grains in Fig. 2b. The shape of CVD grown MoS_2 is determined by the ratio of the molybdenum atoms over Sulphur atoms on the deposition site[18]. If the Mo:S ratio is not equal to 1:1, the shape of CVD grown MoS_2 is triangular[18]. The thickness can be evaluated through Raman spectroscopy by the peak positions of E_{2g}^1 and A_{1g} and the ratio of E_{2g}^1 over A_{1g} as shown in Fig. 2c[12]. Fig. 2d shows the photoluminescence spectra of monolayer MoS_2. There is a sharp peak around 1.8 eV, which is consistent with the fact that the bandgap of monolayer MoS_2 is 1.8 eV[19].

2. 2 Device fabrication of MoS_2-FET

For the device fabrication, synthesized MoS_2 films are transferred onto 90 nm SiO_2/Si substrate. The shapes of MoS_2 (Fig. 3a～3c) were defined by electron-beam lithography followed by an 80 seconds XeF_2 etching. First, a layer of MMA copolymer was spin-coated on a SiO_2 (90 nm)/Si (n^{++}) substrate carrying MoS_2 samples, and then baked on a heating table at 120 ℃ for 2 minutes. After that, another layer of PMMA was spin coated on the substrate, and then baked at 120 ℃ for 10 minutes. The drain and source are defined by electron beam lithography. After the conventional development process, a Ti/Au metal layer (Ti: 10 nm, Au: 100 nm) is deposited by electron beam evaporation to form a source-drain electrode. Finally, acetone is used for the stripping process.

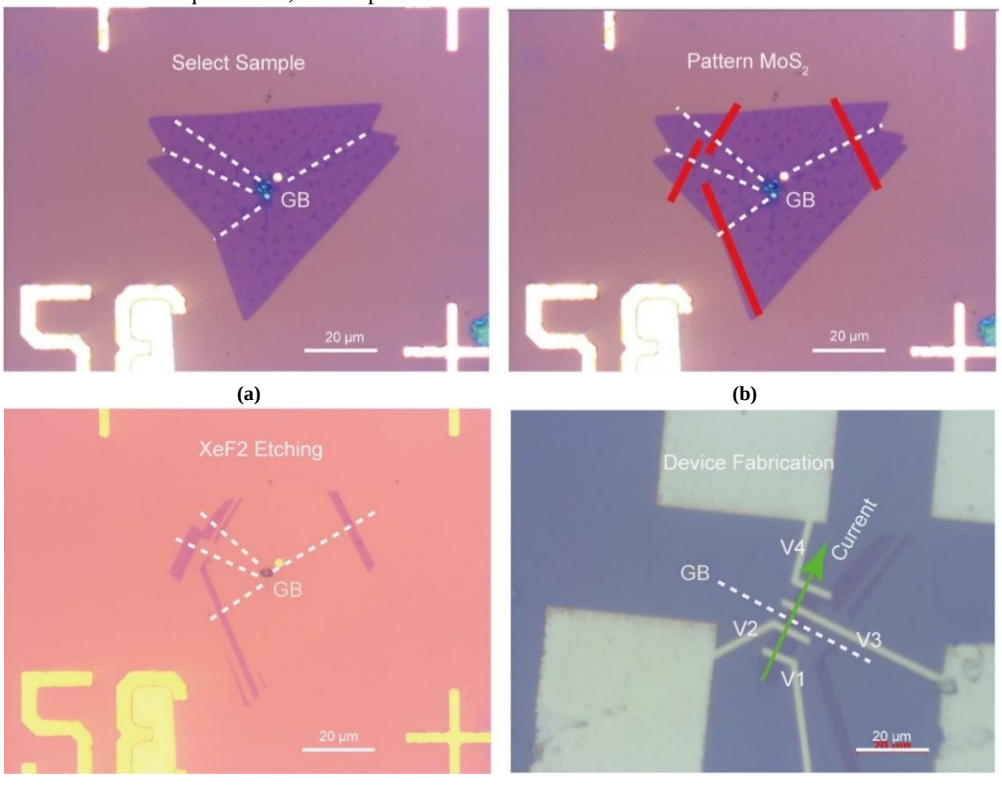


Fig. 3. Device fabrication flow. (a) Selection of grain boundary using optical microscope. White dashed lines show the GBs. (b) MoS_2 ribbons are defined by electron-beam lithography. Red lines indicate the MoS_2 ribbons which are perpendicular to the GBs. (c) MoS_2 was etched by XeF_2 for 80 seconds. The purple area is the remaining MoS_2 after XeF_2 etching. (d) Optical microscope images of fabricated MoS_2 FET with Ti contact on SiO_2 (90 nm)/Si (n^{++}). Ti (10 nm) and Au (100 nm) are used as contact metals

2. 3 Characterization

The thickness of MoS_2 film is identified using optical microscope and AFM (Fig. 2a∼2d), indicating that the sample thickness is 0.75 nm. At the same time, a significant decrease in the thickness at the grain boundaries was observed. Raman spectra are depicted in Fig. 2e and photoluminescence spectra in Fig. 2f. Fig. 4 shows the detailed information of our back-gated monolayer MoS_2-FET device fabrication. The source and drain contacts are Ti/Au (10 nm/100 nm) deposited by electron beam evaporation. For four point measurements, current (I) flows from $V1$ to $V4$, and the voltages are measured on $V2$ and $V3$. Hence, channel resistance can be extracted as ($V2$-$V3$)/I. All of the devices are annealed at 5×10^{-6} mbar, 420 K for 2 hours to reduce contact resistance and remove absorbed moisture. All the measurements are carried out at room temperature. Before annealing, MoS_2-Ti contact showed clear Schottky contact behavior. After annealing, MoS_2-Ti contact exhibits an ohmic contact confirmed by the linear behavior of I_{ds}-V_{ds} curves, as shown in Fig. 4b and 4d, respectively. The devices compared in this work are fabricated on the same MoS_2 flakes to reduce variations. All GBs in this work are designed perpendicular to the current flow direction to study the worst-case situation.

3 RESULTS AND DISCUSSION

Figs. 4a and 4c show the transfer curves of back-gated MoS_2-FETs. They clearly display *n*-type behavior, which is consistent with most of CVD MoS_2 FETs. The ON/OFF ratios of the two types of MoS_2-FETs are in the range of 10^7 ∼10^8, which is comparable to the MoS_2-FETs fabricated on exfoliated samples[19]. However, the ON-current is lower than that of FETs fabricated on exfoliated natural MoS_2 samples because of the doping effect[19]. The natural MoS_2 is usually doped by various halogen elements, resulting in an n type doping effect. Compared with the natural MoS_2 sample, CVD synthesized MoS_2 has less dopants because of using high purity sulphur and MoO_3. Hence, the CVD MoS_2 has less impurities, which leads to a high carrier mobility and low current. As shown in Fig. 4b, d, both sets of the I_{ds}-V_{ds} curves of MoS_2-FETs display linear behavior, indicating that the contact is nearly ohmic in nature. It has been shown that Ti can transfer electron to a clean MoS_2 surface to form a nearly ohmic contact. However, the MoS_2-FET without grain boundary in the channel displays a 30% larger ON-current than that of the MoS_2-FET with a grain boundary in the channel (Figs. 4b and 4d).

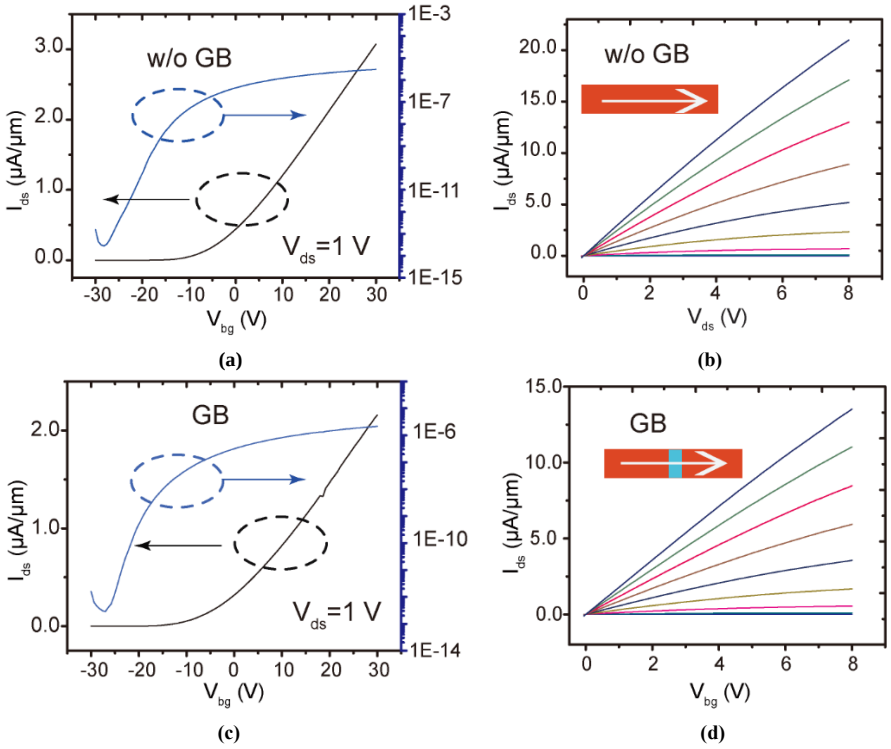
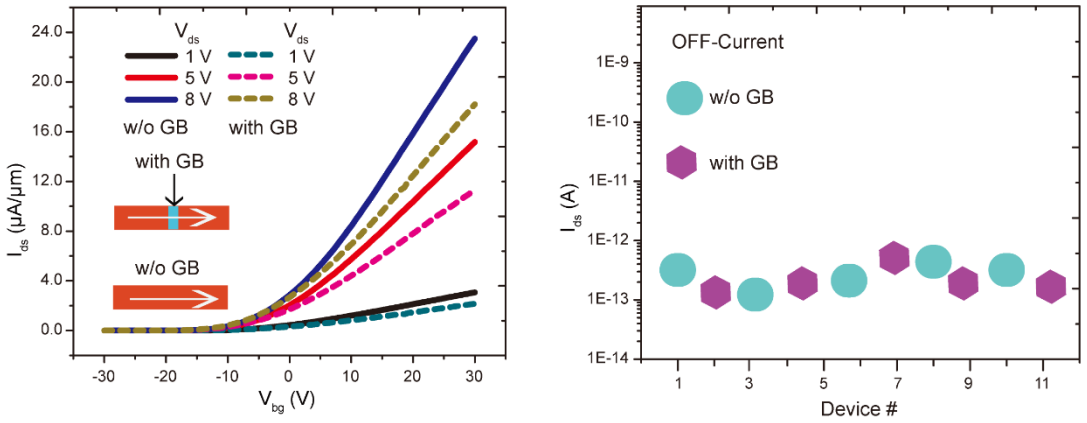


Fig. 4. I_{ds}-V_{bg} curves of monolayer MoS_2-FET with current plotted in both linear (left) and logarithmic (right) scales (a) without GB (w/o GB) in the channel and (c) with GB in the channel. (b), (d) corresponding I_{ds}-V_{ds} curves of (a) and (c), respectively

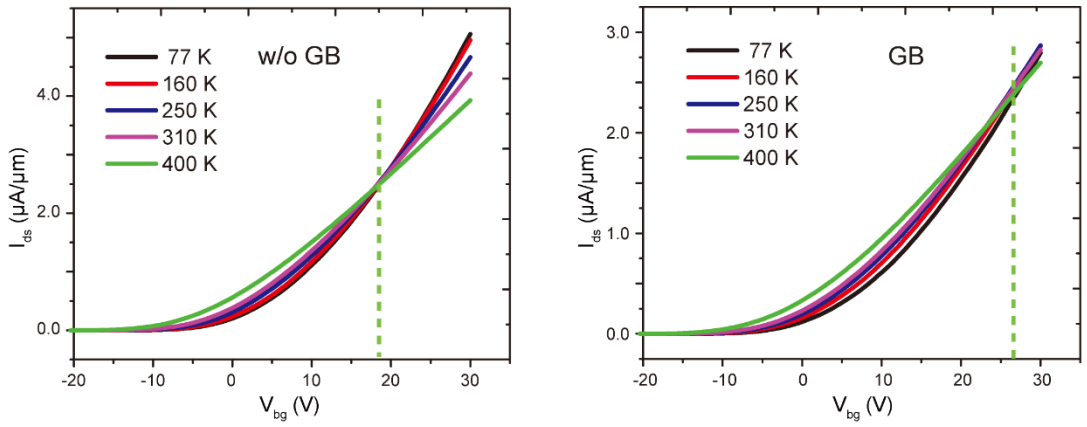
The ON-current is 23.5 μA/μm (V_{ds} = 8 V, V_{bg} = 30 V) on the long channel (L = 8 μm) back-gated MoS_2-FET without a grain boundary (Fig. 4b). However, the ON-current of FET (L = 8 μm) with a grain boundary in the channel is reduced to 15.2 μA/μm (V_{ds} = 8 V, V_{bg} = 30 V), as shown in Fig. 4d and Fig. 5a, indicating that the grain boundary can significantly reduce the ON-current by introducing extra scatterings. On the other hand, from our analysis of many devices, no clear evidence of grain boundary influence on the OFF-current could be identified (Fig. 5b). This is likely due to the fact that the OFF-current levels of all our devices are very low — in the range of 10^{-12} to 10^{-14} A.



(a) **(b)**

Fig. 5. (a) I_{ds}-V_{bg} curves of MoS_2-FET without GB (solid lines) and with GB (dashed lines). (b) Statistics of the OFF-current of the MoS_2-FETs

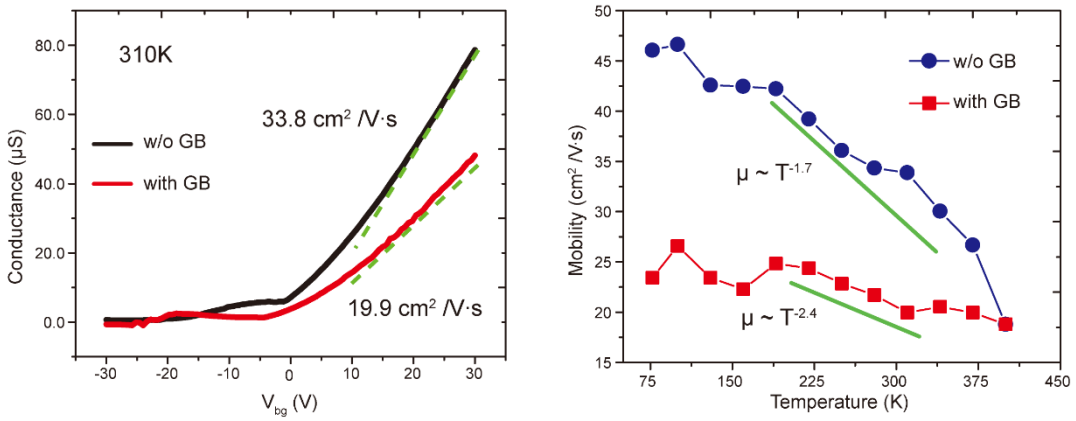
Fig. 6 shows the temperature dependent current of a device as a function of back gate voltage. Without influence of grain boundary, MoS_2 FETs show a clear metal-insulator transition (MIT) like behavior[21]. Note that most of the MIT characteristics have been observed on exfoliated samples. Hence, the observation of MIT phenomenon on our CVD sample indicates that our CVD sample has high quality. When V_{bg} < 18 V, monolayer MoS_2 behaves as a classical semiconductor with conductance increasing with temperature rise due to the increased thermal generation of carriers. For V_{bg} > 18 V, the conductance decreases with increasing temperature, indicating metallic behavior (Fig. 6a). For MoS_2 with grain boundary in the channel, this crossover point occurs at higher V_{bg} (V_{bg} > 26 V, Fig. 6b), because the grain boundary has greater impact on the carrier transport at low temperature, which leads to the faster decrease of the current at low temperature with respect to the high temperature condition.



(a) **(b)**

Fig. 6. Current as a function of gate voltage for different temperature. (a) Without grain boundary in the channel, (b) With grain boundary influence. MoS_2-FETs exhibit a clear MIT behavior. When V_{bg} < 18 V, monolayer MoS_2 behaves like a semiconductor with conductance increasing with temperature. For V_{bg} > 18 V, the conductance decreases with increasing temperature, indicating metallic behavior. For MoS_2 with grain boundary in the channel, this crossover point occurs at higher V_{bg} (V_{bg} > 26 V, Fig. 6b). V_{ds} = 1V for both plots

The field effect mobility of MoS_2 can be extracted as $\mu = (L/W)dG/dV_{bg}C_{ox}^{-1}$. At 310 K, our synthesized long channel (L = 8 μm) MoS_2-FET without a grain boundary shows high quality with a mobility of 33.8 $cm^{-2}/V{\cdot}s$ which is higher than most reported values[5-7, 22]. However, in a long channel device (L = 8 μm) with a GB, the mobility of the device decreases to 19.9 $cm^{-2}/V{\cdot}s$ (Fig. 7a). The plot of the mobility as a function of temperature reveals that grain boundary can significantly reduce the mobility. Besides impurity and phonon scattering, grain boundary is another factor contributing to the mobility degradation and is rather significant. This point has also been confirmed by the analysis of the temperature dependence of the mobility damping factor γ ($\mu \sim T^{-\gamma}$), as shown in Fig. 7b. Above 100 K, mobility damps with a power law with a temperature dependence of $\mu \sim T^{-\gamma}$. With grain boundary, MoS_2-FET displays a lager γ factor of 2.4 than that of MoS_2-FET without grain boundary, indicating that grain boundary can induce extra scattering to further reduce the mobility.



(a) **(b)**

Fig. 7. (a) Channel conductance (G) of MoS_2-FET without grain boundary (black line), and with grain boundary (red line) measured at 310 K by 4-probe method. (b) Intrinsic mobility of MoS_2 of FETs without grain boundary (blue), and with grain boundary (red line) as a function of temperature

4 CONCLUSION

In summary, in this paper, we report the first systematic study of the effects of hybrid grain boundaries on the performance of CVD synthesized monolayer MoS_2-FETs. Our results reveal that grain boundaries play a decisive role in determining the carrier mobility and performance of MoS_2-FETs. In the ON-state, if current flows across a grain boundary that is aligned perpendicular to the channel length, the current can be significantly reduced, while in the OFF-state, the effect is negligible. Metal-insulator-transition is clearly observed, indicating the high quality of our CVD samples, and it is also shown that grain boundaries increase the metal-insulator-transition crossover-voltage in MoS_2-FETs. Thereby, this work provides useful information and guidance in understanding the nature of carrier transport in synthesized MoS_2 devices, and the developed framework can be applied to other 2*D* semiconductors in general, as well as in optimizing the CVD process and device design with 2*D* materials.

REFERENCES

(1) Radisavljevic, B.; Radenovic, A.; Brivio, J.; Giacometti, V.; Kis, A. Single-layer MoS_2 transistors. *Nat. Nanotech.* **2011**, 6, 147–150.

(2) Sarkar, D.; Xie, X.; Liu, W.; Cao, W.; Kang, J.; Gong, Y.; Kraemer, S.; Ajayan, P. M.; Banerjee, K. A subthermionic tunnel field-effect transistor with an atomically thin channel. *Nature* **2015**, 526, 91–95.

(3) Cao, W.; Kang, J.; Sarkar, D.; Liu, W.; Banerjee, K. Performance evaluation and design considerations of 2*D* semiconductor based FETs for sub-10 nm VLSI. *IEEE International Electron Devices Meeting*. New York: IEEE **2014**, p12–14.

(4) Mak, K. F.; Lee, C.; Hone, J.; Shan, J.; Heinz, T. F. Atomically thin MoS_2: a new direct-gap semiconductor. *Phys. Rev. Lett.* **2010**, 105, 136805–6.

(5) Kim, S.; Konar, A.; Hwang, W. S.; Lee, J. H.; Lee, J.; Yang, J.; Jung, C.; Kim, H.; Yoo, J. B.; Choi, J, Y. High-mobility and low-power thin-film transistors based on multilayer MoS_2 crystals. *Nat. Commun.* **2012**, 3, 1011–5.

(6) Wang, H.; Yu, L.; Lee, Y. H.; Shi, Y.; Hsu, A.; Chin, M. L.; Li, L. J.; Dubey, M.; Kong, J.; Palacios, T. Integrated circuits based on bilayer MoS_2 transistors. *Nano Lett.* **2012**, 12, 4674−4680.

(7) Yoon, Y.; Ganapathi, K.; Salahuddin, S. How good can monolayer MoS_2 transistors be. *Nano Lett.* **2011**, 11, 3768−3773.

(8) Shi, Y.; Zhou, W.; Lu, A. Y.; Fang, W.; Lee, Y. H.; Hsu, A. L.; Kim, S. M.; Kim, K. K.; Yang, H. Y.; Li, J. L. Van der Waals epitaxy of MoS_2 layers using graphene as growth templates. *Nano Lett*. **2012**, 12, 2784−2791.

(9) Yu, Y.; Li, C.; Liu, Y.; Su, L.; Zhang, Y.; Cao, L. Controlled scalable synthesis of uniform, high-quality monolayer and few-layer MoS_2 films. *Sci. Rep.* **2013**, 3, 1866−5.

(10) Lee, Y. H.; Yu, L.; Wang, H.; Fang, W.; Ling, X.; Shi, Y.; Lin, C. T.; Huang, J. K.; Chang, M. T.; Chang, C. S. Synthesis and transfer of single-layer transition metal disulfides on diverse surfaces. *Nano Lett.* **2013**, 13, 1852−1857.

(11) Liu, H.; Si, M.; Najmaei, S.; Neal, A. T.; Du, Y.; Ajayan, P. M.; Lou, J.; Ye, P. D. Statistical study of deep submicron dual-gated field-effect transistors on monolayer chemical vapor deposition molybdenum disulfide films. *Nano Lett.* **2013**, 13, 2640−2646.

(12) Lee, Y. H.; Zhang, X. Q.; Zhang, W.; Chang, M. T.; Lin, C. T.; Chang, K. D.; Yu, Y. C.; Wang, J. T. W.; Chang, C. S.; Li, L. J. Synthesis of large-area MoS_2 atomic layers with chemical vapor deposition. *Adv. Mater.* **2012**, 24, 2320−2325.

(13) Zhan, Y.; Liu, Z.; Najmaei, S.; Ajayan, P. M.; Lou, J. Large-area vapor-phase growth and characterization of MoS_2 atomic layers on a SiO_2 substrate. *Small* **2012**, 8, 966−971.

(14) Najmaei, S.; Liu, Z.; Zhou, W.; Zou, X. L.; Shi, G.; Lei, S.; Yakobson, B. I.; Idrobo, J. C.; Ajayan, P. M.; Lou, J. Vapour phase growth and grain boundary structure of molybdenum disulphide atomic layers. *Nat. Mater*. **2013**, 12, 754−759.

(15) van der Zande, A. M.; Huang, P. Y.; Chenet, D. A.; Berkelbach, T. C.; You, Y.; Lee, G. H.; Heinz, T. F.; Reichman, D. R.; Muller, D. A.; Hone, J. C. Grains and grain boundaries in highly crystalline monolayer molybdenum disulphide. *Nat. Mater*. **2013**, 12, 554−561.

(16) Najmaei, S.; Amani, M.; Chin, M. L.; Liu, Z.; Birdwell, A. G.; O'Regan, T. P.; Ajayan, P. M.; Dubey, M.; Lou, J. Electrical transport properties of polycrystalline monolayer molybdenum disulfide. *ACS Nano* **2014**, 8, 7930−7937.

(17) Ly, T. H.; Perello, D. J.; Zhao, J.; Deng, Q.; Kim, H.; Han, G. H.; Chae, S. H.; Jeong, H. Y.; Lee, Y. H. Misorientation-angle-dependent electrical transport across molybdenum disulfide grain boundaries. *Nat. Commun.* **2016**, 7, 10426−4.

(18) Wang, S.; Rong, Y.; Fan, Y.; Pacios, M.; Bhaskaran, H.; He, K.; Warner, J. H. Shape evolution of monolayer MoS_2 crystals grown by chemical vapor deposition. *Chem. Mater*. **2014**, 26, 6371−6379.

(19) Liu, W.; Kang, J.; Cao, W.; Sarkar, D.; Khatami, Y.; Jena, D.; Banerjee, K. High-performance few-layer-MoS_2 field-effect-transistor with record low contact-resistance. *IEEE International Electron Devices Meeting*. New York: IEEE **2013**, p24−27.

(20) Liu, W.; Sarkar, D.; Kang, J.; Cao, W.; Banerjee, K. Impact of contact on the operation and performance of back-gated monolayer MoS_2 field-effect-transistors. *ACS Nano* **2015**, 9, 7904−7910.

(21) Radisavljevic, B.; Kis, A. Mobility engineering and a metal-insulator transition in monolayer MoS_2. *Nat. Mater.* **2013**, 12, 815−820.

(22) Bao, W.; Cai, X.; Kim, D.; Sridhara, K.; Fuhrer, M. S. High mobility ambipolar MoS_2 field-effect transistors: substrate and dielectric effects. *Appl. Phys. Lett.* **2013**, 102, 042104−6.